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# ANALYSIS OF THE CURRENT STATE OF THE ELEMENTS OF TERNARY LOGIC

**Abstract**
***The analysis of the constructed ternary elements and prospects of their development is actual. There are different ways of implementing ternary elements. The problem of development the multivalued logic is the lack of common approach to the implementation of components and elements of non-binary computers. The goal of the work is the comparative analysis the current state of the methods of construction of ternary elements. The history and prospects of development the methods of construction of ternary elements and computer systems on their basis are considered. A comparative analysis of the advantages and disadvantages of such methods of constructing ternary elements as threshold elements of ternary logic based on magnetic elements, ternary elements based on λ-transistor, CMOS transistor and CMOS-C transistors, on binary logic, mathematical models of ternary elements based on neurons, threshold element on bipolar transistors and multithreshold element of multivalued logic according to the main criteria, such as: speed, power consumption, complexity of the structure, the possibility of integrated implementation was made. The future directions of work and expediency of development of subjects of construction of ternary elements and systems on their basis are outlined. All the considered methods of implementation of ternary elements have a number of significant disadvantages. Only using the multithreshold element of multivalued logic allows to create the ternary elements with general approach. One of the obstacles hindering the development of ternary technology is the lack of element base and a common approach to the implementation of components and elements of non-binary computers. Implementing ternary devices based on threshold logic is a way to create ternary devices that can compete with binary devices in terms of equipment.***
***Keywords: ternary logic, multivalued logic, methods of construction of ternary elements, threshold element, multithreshold element of multivalued logic.***

## Introduction

Today, computer technology is evolving at a tremendous rate like never before. They are all based on binary logic, which is a natural consequence of the physical characteristics of semiconductors. One and zero - is currently the basis of all computational processes in computers and other "smart" devices. As the size of the transistors further decreases, the technological process of production and control becomes more complicated [1]. Every 24 months, the number of transistors in the CPU chip doubles - this trend is known as "Moore's Law", and it cannot last forever: the scale of elements and connections can be measured in nanometers, and very soon developers will face a number of technical difficulties. We can assume that the technology of integrated circuits due to large investments and many years of effort has been brought to perfection. A breakthrough in this area is possible only with the emergence of radically new ideas that carry promising prospects [2]. Intel has concluded that one

of the possible ways to solve the problem may be to move from binary to more significant systems, including ternary [3].
Ternary logic - logic that uses three meanings of truth: "truth", "untruth", "I do not know". It was proposed by Jan Lukasevich in 1920 [4]. As a rule, the signs "-" and "+" are used to determine the states "false" and "true", the third state corresponds to the value "0", it means a symmetrical number system is used. It is more understandable and closer to human understanding, but also the following sets are very popular: {0, 1, 2}, {- 1, 0, 1}, {0, ½ ,1}, {N, Z, P}. Based on ternary logic, you can build ternary technology and ternary computing systems. The analysis of the constructed ternary elements and prospects of their development is actual. It is necessary to analyze the current state of different ways of implementing ternary elements, which of them were implemented and how, that`s what this article is devoted. **The objectof study** is the process of analysis the current state of the methods of construction of ternary elements and computer systems on their basis. The different ways of construction of ternary elements are aimed to improve the different characteristics. Therefore, the improvement the speed leads to an increase in equipment. **The subjectof study** is the different methods of construction of ternary elements, their advantages and disadvantages.

**Problem statement**

Suppose a list of n inputs is given, each of which can take one of three values. In a way, they are converted into m outputs, each of which can take two values, which together form one or more ternary functions.In contrast to existing approaches, current coding of ternary levels is proposed.This allows you to combine any number of outputs, which forms the total level of the ternary signal.The limitations of this problem are the lack of a common approach to building the element base of ternary systems, and, as a result - the lack of element base, as well as models and methods of building these elements.Using a multi-threshold element of multi-valued logic (MTEML) as a basic will allow you to build the necessary elements of ternary logic and create models and general methods of their construction.
Theseus Logic proposes to use "extended binary" (actually - Ternary) logic, where in addition to the usual values of "true" and "false" there is a separate signal "NULL", which is used for self-synchronization of processes [5]. Several other research groups are working in the same direction.
Let's consider some examples of ternary elements on the basis of which it is possible to implement devices of ternary computer systems.
Back in 1958, the first ternary computing machine "Setun" was built. It was relatively small for computers of that generation and covered an area of 25-30 $m^2$. Due to its sophisticated architecture, it was able to perform 2000-4500 operations per second, had a memory of 162 nine-titrate cells and a storage device on a magnetic drum with a capacity of 36-72 pages of 54 cells each [6]. In many parameters, such as clock speed, range of processed numbers and performance, it is ahead of its binary counterparts.
After "Setun" there were several experimental projects carried out by enthusiasts (such as the American Ternac and TCA2) [7], but these were either very imperfect machines, far from binary analogues, or software emulations on binary "iron". To date, ternary logic has not yet become widespread. The main reason for this is that the use of ternary elements in computers does not yet give any significant advantages over binary: binary elements are mass production; they are simpler and cheaper in cost. Even if a ternary computer, inexpensive and similar in features to a binary computer, were to be built now, it would have to be fully compatible with it.
Known threshold elements of ternary logic on magnetic elements (TETLM), on which computers "Setun" were built [8, 10, 12]. A characteristic feature of TETLM is the representation of ternary values -1, 0, +1 discrete fixed currents -If, 0, +If, execution of threshold functions of ternary logic by algebraic addition of currents (amperes) in the input circuits of elements, the ability to divide ternary values into their two-digit components and make them from these components. TETLM are made based on electromagnetic technology on magnetic cores [9, 11].
Setun's ferrite memory differed from binary computers in that each memory cell could store one of three different values. Memory was a matrix of ferrite rings. On each ring there were three windings

(Fig. 1). This allowed us to write one of the values 0, 1, -1. Access to the matrix is serial, which significantly reduced the speed of reading / writing trit.
Disadvantages of the threshold element of ternary logic on magnetic elements - built on outdated technologies on magnetic cores, as a result of which it has low speed and cannot be implemented by means of modern integrated semiconductor technologies.

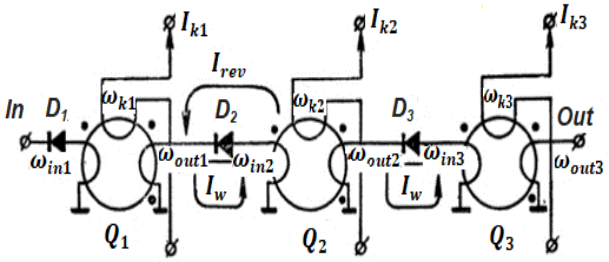


Fig. 1 Ferrite diode logic elements

There have also been attempts to create ternary logic elements on a traditional element base. But the proposed schemes were unattractive, as they consumed energy in static mode. Some sources [13] suggest using a lambda transistor (λ-transistor) to build ternary logic elements (Fig. 2). It is built either on field-effect JFET transistors or on field-effect transistors with a built-in channel. However, the λ-transistor is not able to solve the problem of power consumption by the logic element, as at zero voltage on the base (logic 0), the transistor conducts a significant current.

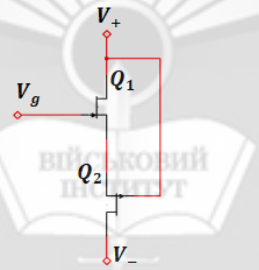


Fig. 2 Scheme of NLT λ-transistor

Some developers have managed to improve the energy-dynamic characteristics of CMOS circuits - their circuits were able to work in a symmetrical ternary system. The ternary element "NO" on CMOS transistors can have a simple implementation as in Fig. 3. But this circuit has a drawback - when the third signal is generated, both transistors must be turned on, this leads to high power consumption. To reduce consumption, it is necessary to complicate the scheme.

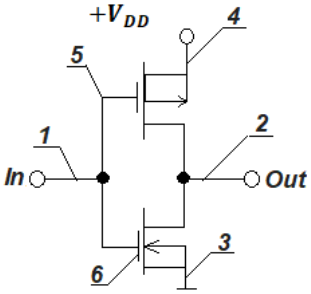


Fig. 3 Ternary element "NO" on CMOS transistors

Fig. 4 shows a circuit of a ternary disjunctor on MOSFETs [14]. The introduction of MOS transistors 8 and 9 with a built-in n-type channel, as well as new structural connections allows you to implement a transistor disjunctor based on ternary logic.

A ternary disjunctor on MOS transistors has two output buses, two n-type induced transistors and two more p-type induced transistors, a resistor, a common positive power bus, a negative power bus, and an output bus.
Disadvantages of these circuits: a large number of transistors in the logic element, complexity, and the use of transistors with high threshold values (created technological difficulties in the manufacture of integrated circuits based on such elements, reduced performance and increased power consumption in dynamic mode).

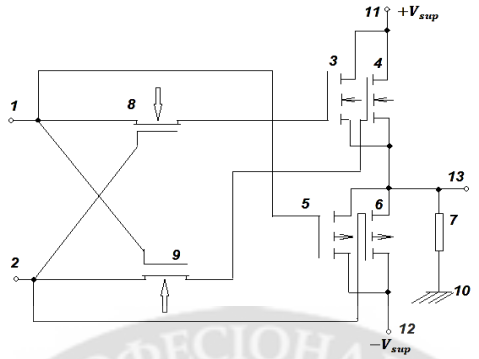


Fig. 4 Ternary disjunctor on MOSFETs

The ternary signal is transmitted by one wire. To encode a logical zero, zero voltage relative to the common point ("ground") is used, to encode a logical "-1" - a negative voltage, and for a logical "+1" - a positive voltage. Thus, a symmetrical power supply with three outputs is required to power ternary logic elements. This ternary basic element on CMOS transistors, in terms of energy-dynamic characteristics and degree of integration, surpasses existing analogues and can be implemented based on standard CMOS technology. However, ternary logic elements based on CMOS-element base are about three times inferior in integration and energy dynamics to binary analogues.
A ternary inverter [14] was also implemented on CMOS transistors, its circuit is shown in Fig.5.

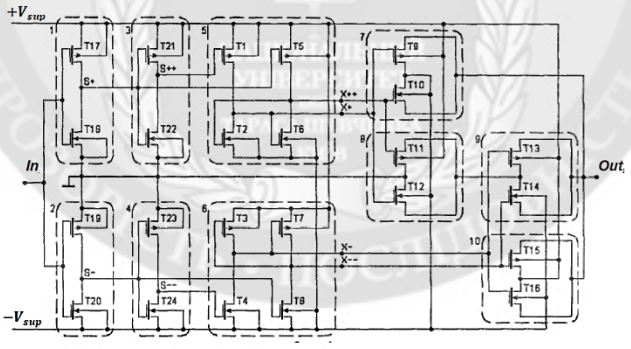


Fig. 5 Scheme of ternary inverter on CMOS transistors

The values of the ternary code "-1" and "+1" correspond to the negative and positive voltages of the bipolar power supply bus, and the values of "0" corresponds to the "ground". The input of the ternary inverter is the input of the control circuit.
The control circuit generates signals for switching the output of the element with the buses of the power supply according to the logical inversion function. With a given logic state at the input, the keys are closed so that the output voltage corresponds to the required value of the ternary code.
By reducing the magnitude of static currents to the values of the leakage currents of the MOS transistors is a decrease in static power consumption in the circuit of the ternary CMOS inverter.

Along with CMOS transistors, there have also been attempts to use CMOS-C transistors. Fig. 6 shows a diagram of the ternary element "OR-NO".

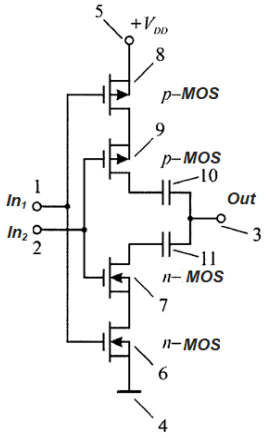


Fig. 6 Ternary element "OR-NO" based on CMOS-C transistors

Due to the introduction of two additional capacitors in the electrical circuit, the first is connected to the drain of the second n-MOS transistor and the output bus, the second to the drain of the second p-MOS transistor and the output bus of the inverter, the leakage of the second p-MOS transistor is connected to the drain of the first p-MOS transistor.

When the low potential of the corresponding state of the logic "-1" to the first input and the second input of the n-MOS transistors 6, 7 are closed, and p-MOS transistors 8, 9 are opened, while the drain of the second p-MOS transistor 10 is a positive the potential (+ Vdd) of the power bus, which through the capacitance of the first capacitor enters the output of circuit 3 and the input of the next logic element, for example, a similar logic element, the gate capacitances of n and p-MOS transistors which form the capacitive load of the logic element.

When applying a high potential corresponding to the state of logic "1", the first and second inputs of the p-MOS transistors 8, 9 are closed, and n-MOS transistors 6, 7 are opened, while on its drain n-MOS transistor 7 is low the potential of the common bus, which through the capacitance of the second capacitor enters the input of the next logic element, which forms a capacitive load.

The gates of the MOS transistors are connected to the input bus. On the surface of the drains and sources of the n-MOS and p-MOS transistors are the corresponding drain electrodes, and the source electrode of the n-MOS transistor is connected to a common bus, and the source electrode of the p-MOS transistor is connected to the power bus. This circuit does not allow more than two logic signal levels (1 bit of information). It should be noted that in this scheme, the drain areas and MOSFET capacitors are functionally integrated. When solving applied problems, an approach is known in which models of ternary devices based on elements of binary logic are used [15]. This method consists in encoding the values of tritium with two bits. For example, a ternary trigger. The basis of the classical binary trigger is a logic circuit consisting of two logical elements of the OR-NO type (Fig. 7.a), which are connected by inverse logical connections. Let us now consider a logical scheme consisting of three logical elements of the OR-NO type (Fig. 7. b).

All logical elements OR-NOT are connected to the neighboring logical elements by means of feedback logical connections, from here 3 logical states follow. Ternary triggers built on binary elements have 2 or 3 logic inputs.

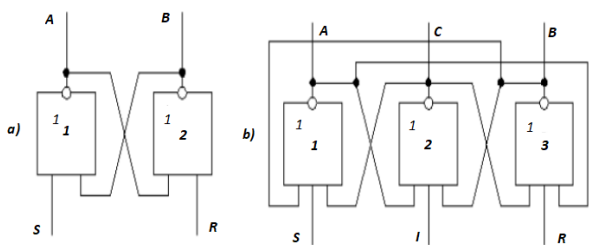


Fig. 7 Triggers on binary elements OR-NO: a) binary trigger; b) ternary trigger

Dual channel triggers are more popular. They have several advantages:
1. Ternary trigger, implemented on the basis of existing binary logic elements.
2. Easy integration with binary devices.
3. Economical implementation: 1 ternary digit consists of 2 binary digits.
To simplify the feedback, use 3 channels, each of which provides 1 logical state. For example, the first channel is logical 1, the second is logical 0, and the third channel is logical -1. Such a circuit may consist of fewer logical binary elements, but it integrates less with existing binary elements and devices built on a 3-channel circuit will have 1.5 times more outputs than when using a 2-channel circuit. The disadvantage of this implementation is the redundancy. To encode 3 states requires 2 elements that can form 4 states. The fourth state is superfluous, but it will be formed.
In addition to potential elements in ternary logic, there are current systems. It is known to implement a ternary logic element on bipolar complementary unsaturated transistors - a threshold element of ternary logic (TETL) [9]. The element is implemented on the basis of a binary ECL-element, the circuit of which is supplemented by its replica on complementary transistors. TETL (Fig. 8) consists of a block of emitter repeaters (BER) and connected to its outputs m blocks of current switches (CS.1… CS.m). BER is implemented on two repeaters, respectively on n-p-n and p-n-p transistors. The first repeater is connected between the common bus and the power bus "-E", the second - between the power bus "+ E" and the common bus. Each CS unit contains 2 current switches. Fixed currents If are formed by two current sources connected to the power buses "+ E" and "-E".

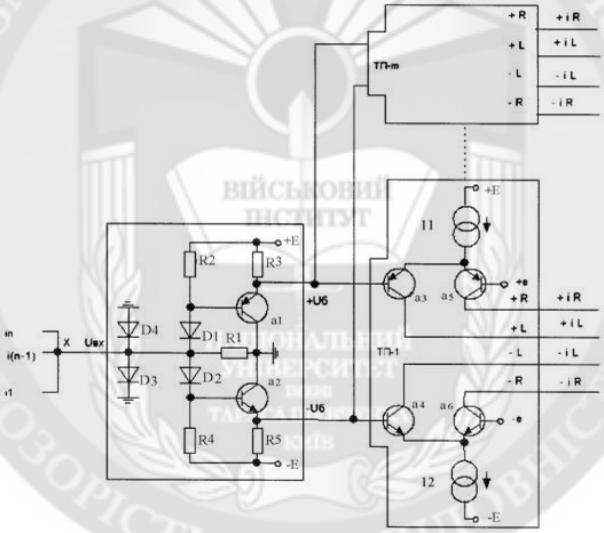

Fig. 8 Threshold element of ternary logic

The input X of the TETL receives n discrete ternary signals. The transformation is performed using the function *tersgn*($n_{+1}$, $n_{-1}$, $n_0$):
*tersgn*($n_{+1}$, $n_{-1}$, $n_0$)=+1, *if* ($n_{+1} - n_{-1}$) > 0,
*tersgn*($n_{+1}$, $n_{-1}$, $n_0$)=0, *if* ($n_{+1} - n_{-1}$) = 0,
*tersgn*($n_{+1}$, $n_{-1}$, $n_0$)= –1, *if* ($n_{+1} - n_{-1}$) < 0,
where:
$n_{+1}$ - the number of signals whose current values are +1,
$n_{-1}$ - the number of signals whose current values are -1,
$n_0$is the number of signals whose current values are 0.
The ternary function tersgn($n_{+1}$, $n_{-1}$, $n_0$) is represented at the outputs of the element by two pairs of its two-valued components - two-bit binary values [+ R, -R] and [+ L, -L]. The correspondence of the components's values to the values of the function *tersgn* ($n_{+1}$, $n_{-1}$, $n_0$) is shown in table. 1 [9].

The connection of the outputs of the element with each other and with the outputs of other elements and the transformation tersgn ($n_{+1}$, $n_{-1}$, $n_0$) provides a set of means by which you can perform on the proposed threshold elements of ternary logic different logic functions.

Table 1

Table of function tersgn ($n_{+1}$, $n_{-1}$, $n_0$)

| tersgn($n_{+1}$, $n_{-1}$, $n_0$) | +R | –R | +L | –L |
|---|---|---|---|---|
| + | + | 0 | 0 | – |
| 0 | 0 | 0 | + | – |
| – | 0 | – | – | 0 |

The disadvantage of TETL is that a small number of thresholds is determined, as a result of which the levels "++" = "0+" and "--" = "0-" do not differ.
However, circuit and structural solutions used in them and tested in practice, can be used in modern digital technology. They are based on a number of ternary elements, such as conjunctors, disjunctors, decoders and triggers. Examples of such devices are shown in Fig. 9

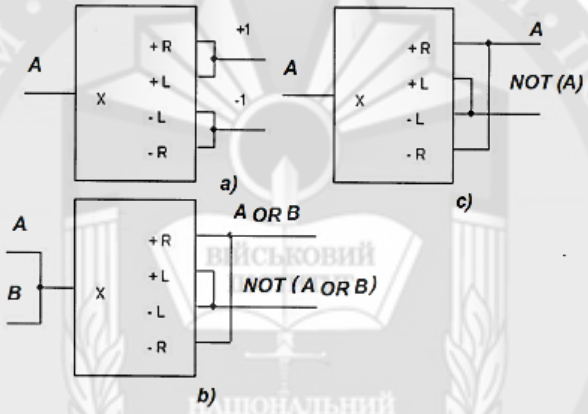


Fig. 9 Elements implemented on the TETL: a) Device for forming constants;
b) Repeater and cyclic inverter of the input variable; c) two-input circuit "OR"

Also, other elements were implemented on the threshold elements, such as an adder [10], and attempts were made to take a systematic approach to the construction of standard elements, for which a node of ternary circuitry, consisting of 3 TETL, was proposed. It can be used to build elements such as triggers. The nodes of this element consist of a TETL and for them everything related to the TETL is valid: the inputs algebraically sum up the Ternary values; nodes can have more than one group of outputs. The implementation of these structures is quite complex and contains many elements.
In addition to the physical implementation of ternary elements, there are systems that use their mathematical model. For example, neural networks on linear and two-threshold neurons that function as a threshold element of ternary logic. There are known examples of construction of such neural networks that implement the elements of minimum, maximum, and ternary inversion [16-18]. Computational intelligence methods combine into hybrid systems various components of intelligent technologies - fuzzy logic, neural networks, genetic algorithms. Hybrid systems, such as fuzzy neural networks with genetic tuning, demonstrate the mutual reinforcement of advantages and disadvantages of individual methods. Today, there are mostly neuro-fuzzy hybrid systems. However, the number of fuzzy genetic, neuro-genetic, and neuro-fuzzy genetic systems is increasing. Schemes of some of them contain not only classical neurons, but also, I, OR neurons. In general, the main task of combining systems of perception and logical processing at the level of structure should be manifested in the fact that there are schemes that work with numbers (perception) and discrete signals of truth

(logic). One of the properties of such logic-oriented hybrid neural networks is their ability to perform complex operations with a simple structure. This, in turn, reduces the number of relationships between elements, which allows you to increase the speed of logical operations. In addition, theoretical research on three-level technology is conducted. It is expected that their results will find their original practical application. Ternary elements of minimum, maximum and inversion in the form of a neural network with linear and two-threshold neurons have been developed. The goal is to increase the efficiency of neural network design. Three neural networks with linear and two-threshold neurons are proposed. The first functions as an element of the ternary maximum, the second as an element of the ternary minimum, and the third as an element of the ternary inversion. The advantages of such solutions are the ability using two-threshold neurons to build neural networks that implement the operations of ternary logic as a separate element [19]. It will also allow to expand the scope of neural networks, to optimize the solution of so-called ternary problems - such as RGB-image processing, three-coordinate problems, etc. It will also combine computer technology with intelligent technology. The disadvantage of this solution can be considered the construction of the actual neural networks on the basis of common binary computers, rather than the construction of the systems themselves, that is, in essence, it is an emulation of ternary elements on a binary basis.

**Materials and methods**

Let`s consider a multi-threshold element of multivalued logic [20] as a basic element for constructing elements of multivalued systems, including ternary. Its block diagram is shown in Fig. 10.

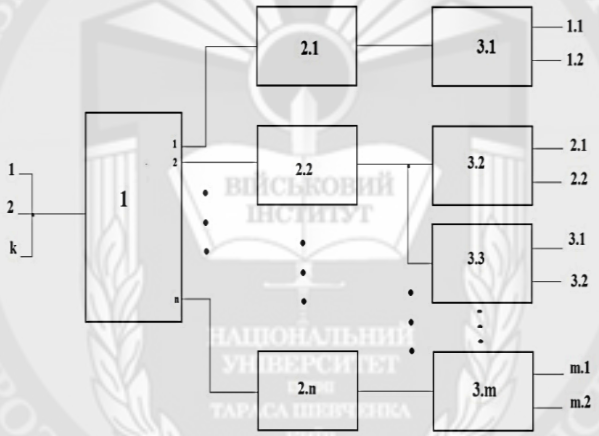


Fig 10 Block diagram of MTEML

Consider in detail its structure and principle of operation. Block 1 is a block of threshold formation (BTF), 2.1… 2.n - emitter repeaters (ER), 3.1 … 3.m - current switches. The input of the threshold formation unit receives k discrete current signals $I_j$ from the previous elements. They can take one of the typical values (for example, for the binary logic of such values will be two: $I_j = +1$, $I_j = 0$; for a ternary symmetric system of such values will be three: $I_j = +1$, $I_j = 0$, $I_j = –1$).

$k = k_{+1} + k_{-1} + k_0$,

where $k_{+1}$ – the number of signals whose current values +1,

$k_{-1}$ – the number of signals whose current values -1,

$k_0$ – the number of signals whose current values 0.

BTF in turn forms n thresholds. Its outputs are fed to the inputs of emitter repeaters (ER) 2.1… 2.n. Active ER generate signals on the connected current switches (CS) 3.1… 3.m.

Features of the structure of MTEML: the element does not operate with potential, but with current values of signals, so the outputs of MTEML can be combined in any number, but the signal can be applied only to the input of one element; ability to form any number of thresholds that MTEML can distinguish. The number of BTF thresholds depends on the number of levels of the input variable that the MTEML is able to distinguish and, accordingly, the bit size of the variable or the complexity of

the operations that can be performed. In order to form the logic of the operation of this element, you need to combine the outputs of the CS in the required combination.
Consider an example of the implementation of MTEML for a ternary symmetric system - its four-threshold version [20], the block diagram of which is shown in Fig. 11.
The electric schematic diagram of the implementation of MTEML with four symmetrical thresholds is shown in Fig. 11.

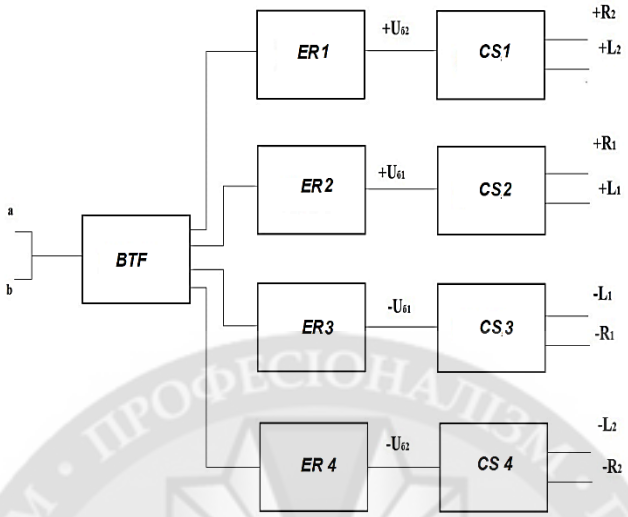


Fig. 11 Block diagram of the four-threshold MTEML

The values of voltages generated at the outputs of the ER and respectively fed to the inputs of current switches are given in table 2. In this table "1" is an active signal (affects the CS), "0" is an inactive signal (does not affect the CS) at the output of the corresponding ER.
If the signal at the input of the CS is active, the output L of the corresponding CS current is generated, otherwise - the current is generated at the output R. CS together have 8 outputs, a combination of which can form the necessary logical or arithmetic functions, as it shown at Fig.12 [20].
The values of the output signals of the SP depending on the input currents are described by the terlev function, given in table. 3.

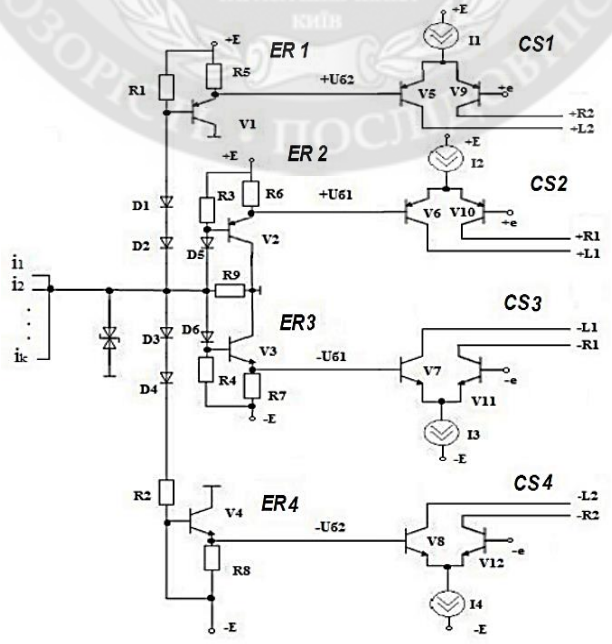


Fig. 12 Electrical schematic diagram of a four-threshold MTEML

The implementation of MTEML for ternary symmetric logic, in comparison with TETL, has several advantages: 4 thresholds of input signals (in TETL - 2), distinguishes 5 levels (in TETL - 3), has 8 output signals (in TETL - 4). All this together allows you to build more diverse logical and arithmetic devices with a simplified implementation [21].

Table 2

Values of voltages at outputs ER1 - ER4

| The sum of the input currents terlev | ER 1($+U_{62}$) | ER 2 ($+U_{61}$) | ER 3 ($-U_{61}$) | ER 4 ($-U_{62}$) |
|---|---|---|---|---|
| – – | 1 | 1 | 0 | 0 |
| – | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 |
| + | 0 | 0 | 1 | 0 |
| + + | 0 | 0 | 1 | 1 |

Table 3

The value of the function terlev

| The sum of the input currents | Output signals of current switches | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | CS1 | | CS2 | | CS3 | | CS4 | |
| terlev | $+R_2$ | $+L_2$ | $+R_1$ | $+L_1$ | –R1 | –L1 | $-R_2$ | $-L_2$ |
| – – | 0 | + | 0 | + | – | 0 | – | 0 |
| – | + | 0 | 0 | + | – | 0 | – | 0 |
| 0 | + | 0 | + | 0 | – | 0 | – | 0 |
| + | + | 0 | + | 0 | 0 | – | – | 0 |
| + + | + | 0 | + | 0 | 0 | – | 0 | – |

**Results**

Having considered in detail the presented methods of implementation of ternary elements, we can compare their main disadvantages and advantages [20].

1. The threshold elements of ternary logic on magnetic elements have serial access, as a result - low speed, memory cells can store one of three states - 0, -1, +1, by means of modern semiconductor technologies cannot be implemented.
2. Ternary elements based on the λ-transistor have high power consumption even in static mode.
3. Ternary elements on CMOS transistors have a very complex structure, many transistors and low speed. The use of CMOS-C transistors leads to the fact that some elements (eg, inverter) allow to have only 2 logic states.
4. Ternary elements built on binary logic have simple integration with binary counterparts, but a lot of feedback connections and redundancy.
5. The threshold element on bipolar transistors provides reliable signal generation, but has insufficient thresholds to distinguish some signal levels (eg ++ and 0+).
6. Mathematical models of ternary elements provide high speed, but do not have their own physical implementation, because neural networks are built on binary elements.

7. The using of MTEML for ternary symmetric logic has several advantages: 4 thresholds of input signals distinguish 5 levels, has 8 output signals. Ternary elements on MTEML have a simple structure, average power consumption and high speed. All this together allows us to build more diverse logical and arithmetic devices with a simplified implementation.
8. The using of MTEML for creating the elements of ternary symmetric logic proposed in this paper is what can allow to create full set of ternary elements with one systematic approach.
Summarizing all the mentioned above, we obtain a comparison table (table 4).

Table 4

Comparison of methods for constructing ternary elements

| Method of constructing ternary elements / Parameters | on magnetic elements | based on λ-transistor | on CMOS-C transistors | on binary logic | on bipolar transistors | based on neurons | based onMTEML |
|---|---|---|---|---|---|---|---|
| Possibility of integrated implementation | - | + | + | + | + | + | + |
| potential (p) or current (c) | c | p | p | p | c | p | c |
| speed | low | low | low | high | high | high | high |
| power consumption | big | big | big | average | average | average | average |
| complexity | complex | complex | very complex | very complex | simple | complex | simple |
| the presence of a systematic approach | no | no | no | no | no | no | no |

9. The implementation of ternary devices based on threshold logic is a way to create ternary devices that can compete with binary devices in terms of equipment, capacity, operational capabilities, speed, and variety.
10. These advantages are significant in such areas as intelligent data processing systems, expert systems, decision theory, i.e., where data analysis is performed.

**Conclusions**

The analysis of the construction of multivalued logic and its elemental base allowed us to draw the following conclusions. All considered examples of realization of ternary elements have rather sufficient lacks:

- threshold elements on magnetic cores use outdated technology, and cannot be implemented with the help of modern integrated technologies;
- the threshold element on bipolar transistors determines a small number of thresholds, as a result it does not distinguish some levels;
- devices on CMOS transistors do not have a standard approach to the implementation of ternary logic;
- elements on binary logic have a rather complex structure and cannot implement a ternary system at the required level;

• implementing ternary elements using a mathematical neural network model is essentially emulating ternary elements on binary computers.

Thus, all these solutions either do not allow the full implementation of ternary logic, or do not have a common approach to its implementation or complicate the implementation of ternary devices and their structure. Therefore, the key topical issue is the development of a standard approach and methods for the synthesis of ternary elements.

One of the obstacles hindering the development of ternary technology is the lack of element base and a common approach to the implementation of components and elements of non-binary computers. Implementing ternary devices based on threshold logic is a way to create ternary devices that can compete with binary devices in terms of equipment.

A topical scientific and practical task is to create a general approach to the implementation of ternary nodes and methods of synthesis of ternary logical and arithmetic elements, as there are still no standards in the development and implementation of ternary elements and a united methodological approach. To build ternary computing and intelligent systems, it is necessary, first of all, to develop the principles of a systematic approach to the synthesis of ternary elements and software for their interaction with each other and with existing modern devices.

Therefore, in further research it is expedient to consider methods of construction and synthesis of nodes of ternary computer systems, their optimization, and development of principles of mathematical modeling and software of such systems and their elements.

**The scientific novelty** of obtained results is that the comparison between different methods of construction the ternary elements is firstly performed. Using the methods of construction the ternary element based on MTEML is proposed both universal and economical. This reduces the amount of equipment.

**The practical significance** of obtained results is that the multithreshold element of multivalued logic allows us to use it for synthesis basic elements of ternary logic and use one approach for all of them. Additional practical advantage is that in practice it allows you to build more diverse logical and arithmetic devices with a simplified implementation.

**Prospects for further research** are to use the method of construction and synthesis of nodes of ternary computer systems, based on MTEML.Their optimization, and development of principles of mathematical modeling and software of such systems and their elements is expedient.

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## АНАЛІЗ СУЧАСНОГО СТАНУ ЕЛЕМЕНТІВ ТРІЙКОВОЇ ЛОГІКИ

***Актуальним є аналіз побудованих потрійних елементів та перспектив їх розвитку. Існують різні способи реалізації потрійних елементів. Проблемою розробки багатозначної логіки є відсутність єдиного підходу до реалізації компонентів і елементівне бінарних ЕОМ. Метою роботи є порівняльний аналіз сучасного стану методів побудови потрійних елементів. Розглянуто історію та перспективи розвитку методів побудови потрійних елементів та обчислювальних систем на їхоснові. Проведено порівняльний аналіз переваг та недоліків таких методів побудови потрійних елементів, як порогові елементи потрійної логіки на основі магнітних елементів, потрійні елементи на основі λ-транзистора, CMOS транзистора та CMOS-C транзисторів, на двійковій логіці, математичні моделі потрійних елементів на основі нейронів, пороговий елемент на біполярних транзисторах та багатопороговий елемент багатозначної логіки за основним икритеріями, такими як: швидкість, енергоспоживання, складність структури, можливість комплексної реалізації. Окреслено майбутні напрямки роботи та доцільність розвитку тематики побудови потрійних елементів і систем на їх основі.***

***Усі розглянуті способи реалізації потрійних елементів мають ряд істотних недоліків. Тільки використання багато порогового елемента багатозначної логіки дозволяє створювати***

***трійкові елементи із загальним підходом. Однією з перешкод, що гальмують розвито ктрійкової технології, є відсутність елементної бази та єдиного підходу до реалізації компонентів та елементів небінарних ЕОМ. Реалізація трійкових пристроїв на основі порогової логіки є способом створення трійкових пристроїв, які можуть конкурувати з двійковими пристроями з точки зору обладнання.***

***Ключові слова: трійковалогіка, багатозначна логіка, методи побудови трійкових елементів, пороговий елемент, багатопороговий елемент багатозначної логіки.***